WHAT IS CLAIMED IS:

1. A circuit having:

an input for receiving an input signal containing a plurality of bits at an input frequency and for receiving a representation of desired output frequency;

a splitter for splitting the input signal into a plurality of split signals each at a frequency of the desired output frequency;

a plurality of catchers for identifying valid bits of a respective split signal;

a shifter for shifting valid bits identified by at least some of the catchers by a predetermined number; and

an output responsive to the shifted valid bits to provide an output signal containing a plurality of valid bits of the input signal at the desired output frequency.

2. The circuit of claim 1, wherein the output is further responsive to the shifted valid bits to derive the predetermined number.

3. The circuit of claim 1, wherein each catcher provides bits of a respective split signal and a valid signal identifying bits of the respective split signal that are valid, and the first-named shifter shifts the respective split signal, the circuit further including a second shifter for

shifting the valid signal identified by at least some of the catchers by the predetermined number.

4. The circuit of claim 3, wherein the output is further responsive to the shifted valid bits to derive the predetermined number.

5. The circuit of claim 1 operating as a phase shifter, wherein the predetermined number is 1.

6. The circuit of claim 1 operating as a frequency reducer, wherein the predetermined number is greater than 1 and identifies a width of the output signal.

7. The circuit of claim 1, wherein the number of split signals and the number of catchers are based on an empirically-derived split factor.

8. The circuit of claim 7, wherein the split factor is based on the input frequency and the desired output frequency.

9. A computer useable medium having a computer readable program embodied therein for addressing data to convert a high frequency data stream to a low frequency data stream at a desired output frequency, the computer readable program comprising:

first computer readable program code for causing the computer to split the high frequency data stream into a plurality of split signals each at a frequency of the desired output frequency;

second computer readable program code for causing the computer to identify valid bits of a respective split signal;

third computer readable program code for causing the computer to shift identified valid bits by a predetermined number; and

fourth computer readable program code for causing the computer to output an output data stream containing a plurality of valid bits of the input signal at the desired output frequency.

10. The computer useable medium of claim 9, wherein the fourth computer readable program code is further responsive to the shifted valid bits to derive the predetermined number.

11. The computer useable medium of claim 9, wherein the second computer readable program code causes the computer to provide bits of a respective split signal and a valid signal identifying bits of the respective split signal that are valid, and the first computer readable program code cause the computer to shift the respective split signal, the computer readable program further including

fifth computer readable program code for causing the computer to shift the valid signal by the predetermined number.

12. The computer useable medium of claim 11, wherein the fourth computer readable program code is further responsive to the shifted valid bits to derive the predetermined number.

13. The computer useable medium of claim 9, wherein the number of split signals is based on an empirically-derived split factor.

14. The computer useable medium of claim 13, wherein the split factor is based on the input frequency and the desired output frequency.

15. A process of converting a phase or frequency of an input data stream to desired output phase or frequency comprising:

splitting the input data stream into a plurality of split signals each at a frequency of the desired output frequency;

identifying valid bits of a respective split signal;

shifting identified valid bits by a predetermined number; and

output an output data stream containing a plurality of valid bits of the input signal at the desired output frequency.

16. The process claim 15, further including deriving the predetermined number from the shifted valid bits.

17. The process of claim 15, further including deriving a valid signal identifying bits of the respective split signal that are valid, and shifting the valid signal by the predetermined number.

18. The process of claim 15, wherein the number of split signals is based on an empirically-derived split factor.

19. The process of claim 18, wherein the split factor is based on the input frequency and the desired output frequency.

20. The process of claim 15, further including selecting a predetermined number to selectively reduce the frequency of the input data stream to an output data stream having a width based on the predetermined number or to shift a phase of the input data stream to the output data stream.